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| 10/500,279 | 01/26/2005 | Alois Stelzl | P04,0213 | 9241 |
| 26574 | 7590 | 02/13/2007 | | |
| SCHIFF HARDIN, LLP PATENT DEPARTMENT 6600 SEARS TOWER CHICAGO, IL 60606-6473 | | | EXAMINER THAI, LUAN C | |
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| SHORTENED STATUTORY PERIOD OF RESPONSE | MAIL DATE | DELIVERY MODE | | |
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Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

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Office Action Summary

Application No.

10/500,279

Applicant(s)

STELZL ET AL.

Examiner

Luan Thai

Art Unit

2891

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☐ Responsive to communication(s) filed on ____.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 21-40 is/are pending in the application.
- 4a) Of the above claim(s) ____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) ____ is/are allowed.
- 6) ☒ Claim(s) 21-37 and 40 is/are rejected.
- 7) ☒ Claim(s) 38 and 39 is/are objected to.
- 8) ☐ Claim(s) ____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 6/28/04 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some * c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. ____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☒ Information Disclosure Statement(s) (PTO/SB/08)
Paper No(s)/Mail Date 6/28/04.
- 4) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date. ____.
- 5) ☐ Notice of Informal Patent Application
- 6) ☐ Other: ____.

DETAILED ACTION

Priority

1. Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

Information Disclosure Statement

2. The Information disclosure Statement filed on 6/28/04 has been considered.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

4. Claims 21, 23, 26-28, 31, 33, 36-37 and 40, are rejected under 35 U.S.C. 102(e) as being anticipated by Stelzl et al (6,838,739).

The figures and reference numbers referred to in this office action are used merely to indicate an example of a specific teaching and are not to be taken as limiting.

Regarding claims 21-23, 26-28, 31, 33, 36-37 and 40, Stelzl et al (see specifically figure 1) disclose a method for production of an encapsulated encapsulation for an electrical component comprising the steps of attaching a plurality of surface wave components (6) (Col. 2, line 66 and

Col. 4, line 60) with metallization fashioned on a plurality of chips (1) to a substrate (2) that has electrical connection areas (10) so that the surfaces of the chips bearing component structures face the substrate and bump connections (5) electrically connect the metallization (4) of the substrate with the connection areas (9) provided on the chips provide a slight distance from the substrate; applying a material (15) to cover at least the lower edges of the chips and a region of the substrate abutting the edges of the chips; applying a first, continuous metal foil layer (11) on the back side of the chips (1), on the material (15) and on edge regions of the substrate (2) abutting the material; and applying a second, hermetically sealing copper foil layer (12) by a solvent-free process or sputtering process (Col. 2, lines 17+) at least on the regions of the first metal foil layer (11) that cover the material (15), wherein the step of providing the metal foil provides a metal foil having contours of the first metal layer so that it lies on the first metal layer with a positive fit (see Fig. 1). Stelzl et al. further teach the step of applying the material applies a plastic film on the back side of the chips to cover the back side, the edges of the chip and subsequently seals the film with the substrate in the entire edge region around the chip (Col. 3, lines 60+). Stelzl et al. also teach the plurality of components after inventively covered are subsequently separated by sawing at a parting location (16) between the soldered-on component substrates (Col. 4, lines 41+).

5. Claims 21-24, 26-28, 31, 36-37 and 40, are rejected under 35 U.S.C. 102(e) as being anticipated by Bureau et al (6,492,194).

The figures and reference numbers referred to in this office action are used merely to indicate an example of a specific teaching and are not to be taken as limiting.

Regarding claims 21-24, 26-28, 31, 36-37 and 40, Bureau et al. (see specifically figures 2-5) disclose a method for production of an encapsulated encapsulation for an electrical component comprising the steps of attaching a plurality of surface acoustic wave components (6) (Col. 1, line 8+) with metallization fashioned on a plurality of chips (10) to a substrate (20) that has electrical connection areas (201/202) so that the surfaces of the chips bearing component structures face the substrate and bump connections (105/106) electrically connect the metallization (101/102) of the substrate with the connection areas (103/104) provided on the chips provide a slight distance from the substrate; applying a material (40), which is a plastic film (Col. 3, lines 51+) on the back side of the chip (10), to cover the back side, the edges of the chips and subsequently sealing the film with the substrate (20) in the entire edge region around the chip; applying a first, continuous metal foil layer (60) on the back side of the chips (10), on the material (40) and on edge regions of the substrate (20) abutting the material; and applying a second, hermetically sealing metal film (80) containing metal particles (Col. 3, lines 1+) by a solvent-free process or sputtering process (Col. 2, lines 17+) on first metal foil layer (60) that cover the material (40) then melting the particles by heating process (Col. 2, lines 58+) onto the first metal layer (60), wherein the step of providing the metal foil provides a metal foil having contours of the first metal layer so that it lies on the first metal layer with a positive fit (see Fig. 5). Stelzl et al. further teach that the plurality of components after inventively covered are subsequently separated by sawing to individualize the packaged electronic components (Col. 2, lines 53+ and Col. 4, lines 43+).

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

7. Claims 32-35 are rejected under 35 U.S.C. 103(a) as being unpatentable over Bureau et al (6,492,194) in view of Alcoe et al. (6,740,959).

The figures and reference numbers referred to in this office action are used merely to indicate an example of a specific teaching and are not to be taken as limiting.

Regarding claims 32-35, Bureau et al discloses the claimed invention as detailed above except for specifying the materials (e.g., titanium, copper and tin) of making the first and second metal layers.

It should be noted that such claimed materials (e.g., titanium, copper and tin) are widely used in the art since they provide better shielding the electronic component from the emissions of electromagnetic interference. For instance, Alcoe et al. teach titanium, copper, tin, alloys of these materials, and composites of these materials being used for making the cover (48) to shield the electronic component (42) from the emissions of electromagnetic interference (Col. 6, lines 59+ and Col. 7, lines 40+). Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to modify Bureau et al by using titanium, copper, tin, alloys of these materials to form first and second metal cover layers, as taught by Alcoe et al., for providing better shielding the electronic component from the emissions of electromagnetic interference. Since tin-copper alloy is assumed in the proposed method of Bureau et al and Alcoe

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et al. for forming the first and second metal layer, the claimed of a melting point greater than 260°C is taken to be inherent for disclosing the same material.

8. Claim 25 is rejected under 35 U.S.C. 103(a) as being unpatentable over Bureau et al (6,492,194) in view of Matsuzawa et al. (6,472,724).

Regarding claim 25, Bureau et al discloses the claimed invention as detailed above except for specifying the material (e.g., metal paste) of the second metal layer.

It should be noted that conductive paste is widely used in semiconductor art to form a shielding layer over the electronic component in order to protect the component from the emissions of electromagnetic interference as disclosed by Matsuzawa et al. (Col. 2, lines 7+). Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to apply metal paste in forming the second electromagnetic shielding layer for the electronic component, since such known material is widely used in semiconductor art, as taught by Matsuzawa, for forming an electromagnetic shielding layer and such application is held to be within the ordinary designing ability expected of a person skilled in the art.

9. Claims 29-30 are rejected under 35 U.S.C. 103(a) as being unpatentable over Bureau et al (6,492,194) in view of Takeuchi et al. (4,711,795).

Regarding claims 29-30, Bureau et al discloses the claimed invention as detailed above except for teaching a cleaning step (e.g., hydrogen plasma) applied on the surface of the first metal layer before forming the second metal layer thereon.

It should be noted that cleaning process, by using hydrogen plasma, is widely used in semiconductor art, as disclosed by Takeuchi et al. (Col. 3, lines 9+), to remove an oxide layer on a surface of a metal layer in order to improve the bonding between such metal layer and another

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metal layer formed thereafter. Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to apply the cleaning step, as taught by Takeuchi et al., to Bureau et al. in order to improve the bonding between the first metal layer and the second metal layer, and such application is held to be within the ordinary designing ability expected of a person skilled in the art.

Allowable Subject Matter

10. Claims 38-39 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

11. The following is a statement of reasons for the indication of allowable subject matter:

The prior art taken either singly or in combination fails to anticipate or fairly suggest, among others, at least the method steps of: sectioning including removing the second metal layer in the regions to be sectioned to expose the first metal layer, chemically etching the exposed regions of the first metal layer to remove the exposed portions and subsequently sectioning by sawing the components apart, as recited in claim 38; especially when these limitations are considered within the specific combination claimed.

12. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Luan Thai whose telephone number is 571-272-1935. The examiner can normally be reached on 8:00 AM - 4:30 PM, Monday to Friday.

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If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Bradley W. Baumeister can be reached on 571-272-1722. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

A handwritten signature in black ink, appearing to read 'Luan Thai', with a long horizontal flourish extending to the right.

Luan Thai

Primary Examiner

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February 6, 2007